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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,276	01/28/2004	Sadami Takeoka	56937-107	7583
20277	7590	05/15/2006		
MCDERMOTT WILL & EMERY LLP 600 13TH STREET, N.W. WASHINGTON, DC 20005-3096			EXAMINER SIEK, VUTHE	
			ART UNIT 2825	PAPER NUMBER

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/765,276	TAKEOKA ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☐ Responsive to communication(s) filed on 28 January 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 15-20 is/are rejected.
- 7) ☒ Claim(s) 5-14 and 21-23 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>1/28/04</u> . | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. This office action is in response to application 10/765,276 filed on 1/28/2004.

Claims 1-23 remain pending in the application.

#### ***Priority***

2. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 1/28/03. It is noted, however, that applicant has not filed a certified copy of the JAPAN P2003-18428 application as required by 35 U.S.C. 119(b).

#### ***Claim Objections***

3. Claims 17, 18, 19 and 20 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The limitation of "A method of simulating..." and "A method of testing..." are not further limited a limitation of a method of evaluating.

Claims 3 and 4 are objected to because of the following informalities: "each of defined delay faults" needed clarification what "defined delay fault" is exactly mean. Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4 and 15-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Iyengar et al., "Delay test Generation 1 – Concepts and Coverage Metrics," IEEE, 1988, pp. 857-866.

6. As to claims 1 and 2, Iyengar et al. teach a method for detecting definite delay faults by computing a threshold (predetermined design delay value). The definite delay faults are detected when delay faults exceed the threshold value (predetermined design delay value) (see abstract, see section 3, page 858-859). This clearly suggests that in order to detect definite delay fault, delay values must be more than the predetermined design delay value or delay values equal to or lower than a predetermined design delay value (threshold) are excluded from a test object. Iyengar et al. teach a new metric called quality metric (see section 4 page 860-861). Iyengar et al. teach a test generator could have a user-specified threshold (predetermined design delay value) for the detection quality, beyond which the fault (delay fault) would be considered adequately detected (see section 5, page 861). Iyengar et al. teach that fault coverage is a ratio of the number of fault detected over the total number of faults (page 860, section 4). From the teachings above, it is clearly suggested that the quality of the test sequences for delay faults (referred to a fault coverage) is a ratio of the number of fault detected (delay faults detected) over the total number of faults (the number of the remaining delay faults to be tested).

7. As to claims 3 and 4, As to claims 1 and 2, Iyengar et al. teach a method for detecting definite delay faults by computing a threshold (predetermined design delay

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value). The definite delay faults are detected when delay faults exceed the threshold value (predetermined design delay value) (see abstract, see section 3, page 858-859). In addition, Iyengar et al. teach faulty waveforms are functions of the variable size delay fault (see page 861). This clearly suggests that in order to detect definite delay fault, delay values must be weighted as delays having values more than the predetermined design delay value. Iyengar et al. teach a new metric called quality metric (see section 4 page 860-861). Iyengar et al. teach a ratio of the total of the weights with respect to the "delay faults detected by the test sequences for delay faults" to the total of the weights with respect to the defined delay faults is set as a fault coverage (see section 4, pages 860-861). The quality of detection is evaluated. Page 861 shows some examples of the ratio. The ratio evaluates the quality of the test sequences for delay faults.

8. As to claims 15 and 16, Iyengar et al. teach calculating a fault coverage (see section 4, pages 860-861).

9. As to claims 17, 18, 19 and 20, Iyengar et al. teach simulating and testing the quality of the test sequences for delay faults to thereby calculating a fault coverage (see section 4, pages 860-861).

#### ***Allowable Subject Matter***

10. Claims 5-6; 7, 11; 8, 12; 9, 13; 10, 14; and 21-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening

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claims and if rewritten to clarify the claim limitations as above claim objections (related to claims 3 and 4).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

  
VUTHE SIEK  
PRIMARY EXAMINER